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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,777	12/31/2001	Deborah T. Marr	042390.P12495	9070

7590 10/06/2004

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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,777	MARR ET AL.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/05/02; 03/19/03;*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *See Continuation Sheet*.

Continuation of Attachment(s) 6). Other: IDS mail date 06/19/03 and 06/18/04.

DETAILED ACTION

Papers Submitted

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Oath/Declaration as received on 04/15/02; Information Disclosure Statement as received on 08/05/02; Information Disclosure Statement as received on 03/19/03; Information Disclosure Statement as received on 06/19/03; and Information Disclosure Statement as received on 06/18/04.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-26 rejected under 35 U.S.C. 102(e) as being anticipated by Kalafatis et al., U.S. Patent Number 6,535,905 (herein referred to as Kalafatis).

Referring to claims 1 and 18 Kalafatis has taught a processor comprising: a memory to store a plurality of program threads (Kalafatis figure 3 number 106);

a plurality of thread partitionable resources that are each partitionable between a plurality of threads (Kalafatis figure 4 numbers 106, 62, 103, retirement logic; column 13 lines 32-38);

a processor coupled to said memory;

logic to receive a program instruction from a first thread of said plurality of threads, and in response to said program instruction to cause the processor to suspend execution of the first thread and to relinquish portions of said plurality of thread partitionable resources associated with the first thread for use by other ones of said plurality of threads (Kalafatis figure 14 figure 8 column 10 lines 25-39, column 18 lines 62-column 19 line 36; switching takes place between threads when a branch instruction occurs, and also at an instruction, or inserted flow, is inserted in the instruction sequence).

Referring to claim 2 Kalafatis has taught wherein the program instruction is a suspend instruction (Kalafatis figure 14, column 18 lines 62-column 19 line 36; switching takes place between threads when an instruction, or inserted flow, is inserted in the instruction sequence).

Referring to claim 3 Kalafatis has taught wherein said logic is to cause the processor to suspend the first thread for a selected amount of time (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-63).

Referring to claim 4 Kalafatis has taught wherein said selected amount of time is a fixed amount of time (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-63; the number is predetermined).

Referring to claims 5 and 19 Kalafatis has taught wherein said processor is to execute instructions from a second thread while said first thread is suspended (Kalafatis column 2 lines 3-12, column 4 lines 10-49).

Referring to claims 6 and 20 Kalafatis has taught wherein said selected amount of time is programmable by at least one technique chosen from a set consisting of:

providing an operand in conjunction with the program instruction; blowing fuses to set the selected amount; programming the selected amount in a storage location in advance of decoding the program instruction; setting the selected amount in microcode (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-column 14 line 6; since the number is predetermined, it is programmable by the control register bus).

Referring to claims 7 and 21 Kalafatis has taught wherein said plurality of thread partitionable resources comprises: an instruction queue (Kalafatis figure 4 number 103); a register pool (Kalafatis column 13 lines 32-46).

Referring to claims 8 and 22 Kalafatis has taught further comprising: a plurality of shared resources, said plurality of shared resources comprising: a plurality of execution units (Kalafatis figure 4 number 70); a cache (Kalafatis figure 4 number 44); a scheduler (Kalafatis figure 4 number 72); a plurality of duplicated resources, said plurality of duplicated resources comprising: a plurality of processor state variables; an instruction pointer; register renaming logic (Kalafatis figure 4 number 76/78, 100) .

Referring to claims 9 and 23 Kalafatis has taught wherein said plurality of thread partitionable resources further comprises: a plurality of re-order buffers; a plurality of store buffer entries (Kalafatis column 13 lines 32-46).

Referring to claim 10 Kalafatis has taught wherein said logic is further to cause the processor to resume execution of said first thread in response to an event (Kalafatis column 8 lines 5-36).

Referring to claim 11 Kalafatis has taught wherein said logic is further to cause the processor to ignore events until said selected amount of time has elapsed (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-63; the number is predetermined).

Referring to claim 12 Kalafatis has taught wherein said processor is embodied in digital format on a computer readable medium (Kalafatis column 1 line 5-column 2 line 15).

Referring to claims 13 and 24 Kalafatis has taught a method comprising:

receiving a first opcode in a first thread of execution;

suspending said first thread for a selected amount of time in response to said first opcode;

relinquishing a plurality of thread partitionable resources in response to said first opcode (Kalafatis figure 14 figure 8 column 10 lines 25-39, column 18 lines 62-column 19 line 36; switching takes place between threads when a branch instruction occurs, and also at an instruction, or inserted flow, is inserted in the instruction sequence);

re-partitioning said plurality of resources after a selected amount of time (Kalafatis column 10 lines 62-column 11 line 19, column 7 lines 8-35).

Referring to claim 14 Kalafatis has taught wherein relinquishing comprises: annealing the plurality of thread partitionable resources to become larger structures usable by fewer threads (Kalafatis column 7 lines 8-35, figure 2).

Referring to claims 15 and 26 Kalafatis has taught wherein relinquishing said plurality of thread partitionable resources comprises: relinquishing a partition of an instruction queue(Kalafatis figure 4 number 103) ; relinquishing a plurality of registers from a register pool (a register pool (Kalafatis column 13 lines 32-46)

Referring to claim 16 Kalafatis has taught wherein relinquishing said plurality of thread partitionable resources further comprises: relinquishing a plurality of store buffer entries; relinquishing a plurality of re-order buffer entries (Kalafatis column 13 lines 32-46).

Referring to claim 17 Kalafatis has taught wherein said selected amount of time is programmable by at least one technique chosen from a set consisting of:

providing an operand in conjunction with the first opcode;

blowing fuses to set the selected amount of time;

programming the selected amount of time in a storage location in advance of decoding the program instruction;

setting the selected amount of time in microcode (Kalafatis column 22 line 66-column 23 line 6, figure 9 box 284, column 13 lines 61-column 14 line 6; since the number is predetermined, it is programmable by the control register bus).

Referring to claim 25 Kalafatis has wherein said first instruction is a macro-instruction from a user-executable program (Kalafatis column 3 line 45-column 4 line 7).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Saville et al., U.S. Patent Number 6,401,155 has taught interrupt process multi-threaded processing with partitioned resources.

Davis et al., U.S. Patent Number 5,357,617 has taught concurrent multiple instruction thread processing with a single pipeline processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579 and 571-272-4167 after 10/12/04. The examiner can normally be reached on 8Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles Allen Harkness

Examiner

Art Unit 2183

September 27, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100